Analog design techniques in Nanometer CMOSA technologies

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Channel lengths of standard CMOS technologies continue to shrink, as predicted by Moore. Consequently, amplifiers and filters require the biasing points of the transistors to move deeper in weak inversion. As a result the speed is reduced considerably. A new design procedure is derived in all three regions of operation i.e. strong and weak inversion and velocity saturation. BSIM6/EKV model parameters are used. Optimum biasing points are derived for single- and two-stage amplifiers. It is shown that for channel lengths close to 20 nm, a unique optimum is achieved for the fT x gm/IDS figure of merit.

At such low channel lengths noise and distortion establish severe limitations in dynamic range. They can be mitigated by the use of negative resistors and bootstrap techniques, as used in an increasing number of amplifier and filter configurations. An overview is given of such circuit configurations.

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